REMARKS

In the Office Action dated September 9, 2006, the Examiner rejected claims 19, 20, 22-27, 33 and 34 under 35 USC 102(e) as anticipated by Kinsman (US Publication 2002/0027257), rejected claims 21, 28-31 under 35 USC 103 as unpatentable over Kinsman, and rejected claims 35-42 under 35 USC 103 as unpatentable over Kinsman, Capote, and Pasadyn (US Patent 6,605,479). Claims 19-43 remain at issue.

THE ART REJECTION

The Examiner rejected certain claims as anticipated by Kinsman. The Applicants disagree. Kainsman does not anticipate the present invention as claimed.

Certain claims of the present invention are directed toward a flip chip integrated circuit having bond pads formed on the active surface and solder balls formed on the bond pads. A substantially uniform layer of underfill adhesive is applied directly onto the active surface of the flip chip and around the solder bumps.

The Kinsman reference does not anticipate the present invention for a number of reasons.

1. In the Kinsman reference, as illustrated in Figures 1A through 1F, the bond pads 12 on the surface of the wafer 10 are bumped with intermediate conductive elements 20. According to various embodiments of Kinsman, the conductive elements 20 are made from one or more metals such as copper, or a copper-chromium alloy, or chromium. See specifically Figures 1A and 1B and paragraph [0023] of the reference. As next described in paragraph [0026] and illustrated in Figure 1C, the encapsulant material 30 is formed across the surface of the wafer, entirely covering conductive elements 20. Once the material 30 is cured, it is then planarized (see figure 1D) by chemical-mechanical polishing, so that a top surface of the elements 20 are exposed. Thereafter, as illustrated in Figure 1E, solder balls 32 are formed on the exposed surfaces of the conductive elements 2. See paragraph [0027].

The structure of Kinsman therefore significantly differs from the present invention as claimed. With the present invention, a substantially uniform layer of underfill adhesive is formed ***around*** the solder bumps formed on the integrated

circuit. In contrast, the Kinsman reference clearly teaches that the solder balls are formed on top of the encapsulant material 30.

2. The Kinsman reference teaches the use of an "encapsulant" material 30. An encapsulant material, however, is not the same as the underfill material as claimed in the present invention. As described in the specification of the present application, the purpose of the underfill material is to reflow when the flip chip is mounted onto a substrate, forming a seal between the chip and substrate. A careful review of the reference, however, indicates that the material 30 of Kinsman is not an underfill material. Paragraph [0026] specifically states that the encapsulant material 30 forms a "hermatic seal" over the integrated circuitry 18 on the active surface 14 of the substrate. Since the stated purpose of the encapsulant 30 is to form a hermatic seal over the circuitry, Kinsman actually teaches away from the present invention. If the material 30 were to reflow like the underfill material of the present invention, there is a strong possibility that the hermatic seal would be broken, exposing the underlying circuitry 18.

For at least the reasons discussed above, the Kinsman reference does not anticipate the claims of the present invention.

Certain other claims have been rejected based on the combination of Capote and Pasadyn. The Applicants strongly disagree. The Examiner has failed to demonstrate a prime facie case of obviousness.

The Capote publication teaches various methods for applying an encapsulant material 22 that is applied using either a liquid that is hardened or an adhesive tape that is applied to a chip.

In Figure 12 for example, the encapsulant material 22 is a film laminated onto a tape. See paragraph [0036].

In the Figure 4 embodiment, the chip 10 is pre-coated with the encapsulant material 22 prior to assembly to the substrate 20. Specifically, the encapsulant is uniformly spread across the surface 16 of the chip 10 between the solder bumps 14. See paragraph [0037].

In the Figure 5 embodiment, the chip 10 is coated with a high temperature thermoplastic adhesive 19 and film 21 (see figure 12), then the contact pads 24 are exposed by making vias through the encapsulant 22 with a laser, plasma or chemical etch, photo-imaging, etc. See paragraph [0038].

Contrary to the Examiner's statements in the rejection, there is no discussion whatsoever in paragraph [0038], or elsewhere in the reference, teaching or suggesting the cutting of the edges of the encapsulant 22.

In the Figure 10 embodiment, the chip 10 is pre-coated with a first film 37 laminated onto the chip 10 while the substrate 20 is pre-coated with a second film layer 39. Together, the first and second films form the encapsulant material 22. See paragraph [0039].

The Capote reference thus teaches the application of either an adhesive tape or a liquid that is applied and hardened onto a surface of a flip chip. Nowhere, however, does Capote teach or suggest a flip chip having a substantially uniform layer of underfill adhesive where the flip chip and the underfill adhesive material, together, form continuous cut edges around the periphery of the flip chip. Capote therefore does not anticipate or suggest the present invention as claimed.

The Pasadyn reference is directed toward a method of identifying operational and defective die on a wafer. Other than both being broadly directed to semiconductors, the Capote and Pasadyn references have absolutely nothing in common. There is absolutely no reason why one of ordinary skill in the art working in the area of flip chip packaging would consider a reference related to the testing of dice on a wafer and vice versa. The two references are therefore not combinable as suggested by the Examiner.

Furthermore, even if it were proper to combine the two references, it still would not result in the present invention as claimed. Instead, the proposed combination would result in the flip chip of Capote that is tested while still in wafer form using the metrology technique as taught by Pasadyn. The proposed combination, however, would not teach a wafer having a partially cured underfill adhesive layer formed on the active surface of a flip chip wafer.

Lastly, the two references actually teach away from one another. The Capote reference explicitly teaches the application of either an adhesive tape or a liquid that is applied and hardened onto a surface of an individual flip chip, whereas the Pasadyn reference is directed to using a metrology tool to identify good and bad die on a wafer. One reference is therefore at the wafer level, while the other is at the chip level. The two references therefore teach away from one another.

Therefore, the Examiner has failed to demonstrate a prima facie case of obvious. The claims rejected based on the combination are therefore allowable.

The Applicants' believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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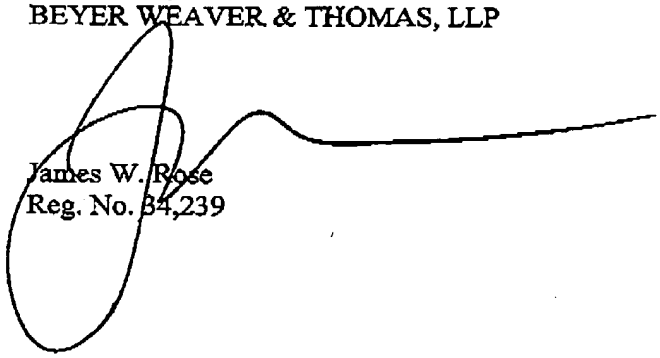

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